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09/703,181	10/30/2000	Michael T. Moore	CY-0016	9600

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	09/703,181	MOORE ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 2/8/2005. Claims 1-23 are pending, wherein claims 10-11 have been amended.

Oath/Declaration

2. It appears that the original copy of the oath or declaration in Applicant's possession (as filed on 10/30/2000) is valid as previously approved by the Examiners. However, the scan-in image of the oath or declaration in the file contains many missing words and un-readable or difficult to read words due to the paper being faxed-in, in slanted position and/or printed in slanted position, which resulted in poor scan-in quality, rendering the oath or declaration defective.

3. Accordingly, Applicant is required to provide a clean copy of the original copy of the Oath or Declaration as filed on 10/30/2000 for compliance with 37 CFR 1.67(a), or alternately, a new oath or declaration in compliance with 37 CFR 1.67(a) (see MPEP §§ 602.01 and 602.02).

Claim Objections

4. **Claim 11** is objected to because of the following informalities:

As per **claim 11**, "may" (line 2) should be deleted to clearly identify what is being claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-3,5-6,9,15-17** are rejected under 35 U.S.C. 102(b) as being anticipated by **Chang** (US Patent No. 5,687,325).

As per **claim 1**, the integrated circuit device (i.e., a single IC chip) with programmable portion (i.e., general purpose FPGA), and the communication portion are described in col. 3, lines 21-55 (see also Figs. 1-2), wherein the FGPA comprising a plurality of circuits configurable by the user (i.e., logic gates--col. 1, lines 35-44), being necessary to perform the desired, custom or specific digital logic functions when configured by the user or designer, either directly or indirectly via computer program (see col. 5, lines 28-65; co. 2, lines 25-30), wherein the communication portions correspond to fixed functional units (i.e., the circuit block manufactured to perform a predetermined data communication function--see col. 5, lines 19-35) such as bus interface, event timers, interrupt controller, DMA controller, system timers, real-time clock, RAM, clock synthesizer, RAM Digital-to-Analog Converter (DAC), display interface, register file, compressed image encoder/decoder (CODEC) which serve as

communication portions between the FPGA and the computer system, wherein the at least one manufactured circuit block including converting received first data values into second data values correspond to at least one of compressed image encoder/decoder (col.7, lines 6-22) and RAM Digital-to-Analog Converter (DAC) (col. 6, lines 53-57).

As per **claim 2**, all of the elements of claim 1, from which the claim depends, are discussed in the rejection of claim 1 above, wherein the programmable portion includes interconnect portion and logic gate portion are part of interconnections and logic gates or configurable blocks as described in col. 1, lines 37-40 as part of the general purpose FGPA (see also col. 5, lines 41-53)

As per **claim 3**, all of the elements of claim 2, from which the claim depends, are discussed in the rejection of claim 2 above, wherein the memory circuit for storing configuration information is inherently included in order to store the configuration data or information being loaded into the FPGA as described in col. 5, lines 54-65.

As per **claim 5**, all of the elements of claim 1, from which the claim depends, are discussed in the rejection of claim 1 above, wherein plurality of input/outputs commonly connected to the programmable portion and the communication portion are illustrated in Figs. 1 and 2, corresponding to I/O busses of blocks 32, 34, 36, 38, 42, 44, 46, 86, 84, 88, 92, 82, 44', 46'.

As per **claim 6**, all of the elements of claim 1, from which the claim depends, are discussed in the rejection of claim 1 above, wherein at least the bus interface, RAM, RAM Digital-to-Analog Converter (DAC), display interface, and compressed image

encoder/decoder (CODEC) are data operation circuits as part of the communication portion and perform a different function on received input data as the names imply.

As per **claim 9**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the operation control store that provides one of a plurality of operational values to the data operation circuits that controls the type of operation performed on the received data, corresponds to at least the register file 72 (see Fig. 2), which receives and stores data which specifies a particular operating mode of the graphic controller (col. 6, line 66 to col. 7, line 5), and at least to the configuration data stored in PROM (col. 5, line 41 to col. 6, line 17) for controlling the various components of the integrated circuit device to perform the specific function.

As per **claims 15-16**, the elements of the claim are discussed in the rejection of claim 1, above, wherein the integrated circuit device (i.e., Application Specific Field Programmable Gate Array "ASFPGA" on a single chip) is implemented as a semiconductor device as is well known in the art for fabricating integrated circuits, wherein the same integrated circuit device of claim 1 can also be equivalently described in the art as programmable logic device having embedded with non-programmable portion (i.e., communication portion with non-programmable or fixed or non-configurable circuits) or vice versa, wherein such communication portion is selectable or configurable by the designer/system builder as discussed in the rejection of claim 1, including having a plurality of circuit blocks that each provides different data communication functions (as per claim 16) (see rejections of claims 1 and 6 above).

As per **claim 17**, all of the elements of claim 16, from which the claim depends, are discussed in the rejection of claim 16 above, wherein the path between each circuit block and a data output is described in the rejection of claim 5, resulting from having common inputs/outputs connections and various buss interfaces, wherein such path is selectable or configurable in accordance to the desired functionality as determined by the system builder (col. 5, lines 28-65; co. 2, lines 25-30).

7. **Claims 1-3,6-7,13-16,18-21** are rejected under 35 U.S.C. 102(e) as being anticipated by **Chang** (US Patent No. 6,260,087).

As per **claims 1-2**, Figs. 1, 2 and 3 illustrate the elements of the claims, wherein the integrated circuit device corresponds to the ASICs 10, 30, 40, wherein the programmable portion corresponds to programmable logic blocks 26, 26' and 26" (see abstract; col. 5, line 33 to col. 7, line 55), wherein since these programmable logic blocks employ Programmable Logic Device (PLD) or FPGA or GAL (col. 7, line 56 to col. 8, line 20), the plurality of configurable circuits, including programmable interconnect portion and logic gate portion (as per claim 2) are inherently included in the PLD or FPGA or GAL structures as is well known in the art, wherein these configurable circuits are configurable by the user or designer in permitting the system builder to make the desired configuration (see col. 4, lines 56 to col. 5, line 8), wherein the communication portion corresponding to at least one of the non-programmable functional blocks 12, 12', 12", 14,14', 14", 16, 18, 18', 18", 27, 27', 28, 28', 28", 22, 32, 44, 46, 48, (see abstract; col. 5, line 33 to col. 7, line 55) wherein the communication portion including converting received first data values into second data values

correspond to at least the up/down frequency converter (44), frequency hopping spread spectrum Mod/Demod (46), baseband A/D-D/A (48), respectively, performing the functions as the names imply (i.e., frequency conversion from first values to second values, frequency modulation/demodulation from first values to second values, analog to digital and digital to analog conversion from first values to second values) (see col. 7, lines 8-55), wherein these non-programmable functional blocks are communication portions in the sense that they are associated with communication among the system components, in terms of providing storage for data transfer or configuration data storage during system setup (i.e., SRAM, EEPROM, flash memory, FIFO), bus interfaces (i.e., PCI bus interface, ISA bus interface, EISA bus interface, Serial Data I/O, USB), processing units for data transfer (i.e., DSP, micro-controller, RISC or CISC, customized logic), and specialized data conversion circuits performed during data transfer (i.e., baseband Analog to Digital Converter - Digital to Analog Converter, frequency hopping spread spectrum Mod/Demod, Up/down frequency converter).

As per **claim 3**, all of the elements of claim 2, from which the claim depends, are discussed in the rejection of claim 2 above, wherein memory circuit for storing configuration information is taught in col. 6, line 66 to col. 7, line 7; col. 7, lines 45-46; col. 6, lines 35-45.

As per **claim 6**, all of the elements of claim 1, from which the claim depends, are discussed in the rejection of claim 1 above, wherein the plurality of data operation circuits, each performing a different function on its received data input, corresponds to at least the up/down frequency converter (44), frequency hopping spread spectrum

Mod/Demod (46), baseband A/D-D/A (48), and the serial input output (SIO) respectively, performing the functions as the names imply (i.e., frequency conversion from first values to second values, frequency modulation/demodulation from first values to second values, analog to digital and digital to analog conversion from first values to second values, and parallel to serial data conversion) (see col. 6, lines 46-67; col. 7, lines 8-55) as discussed in the rejection of claim 1 above.

As per **claim 7**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein at least the SIO block inherently converts parallel data to serial data or vice versa, which involves converting an input data word into an output data word having different bit values (i.e., parallel data transfer have different bits that serial data transfer) than the input data word.

As per **claim 13**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein physical layer circuit providing data output stream compatible with the particular data transmission media corresponds to at least the i/o interface block used, for adapting to the particular bus or busses (i.e., ISA, USA, EISA, bus interface blocks) (col. 5, lines 43-55).

As per **claim 14**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the plurality of communication portions are one of the non-programmable functional blocks 12, 12', 12", 14,14', 14", 16, 18, 18', 18", 27, 27', 28, 28', 28", 22, 32, 44, 46, 48, (see abstract; col. 5, line 33 to col. 7, line 55) as discussed in the rejection of claim 1 above.

As per **claims 15-16**, the elements of the claim are discussed in the rejection of claim 1, above, wherein the integrated circuit device (i.e., Application Specific Field Programmable Gate Array "ASFPGA" on a single chip) is implemented as a semiconductor device as is well known in the art for fabricating integrated circuits, wherein the same integrated circuit device of claim 1 can also be equivalently described in the art as programmable logic device having embedded with non-programmable portion (i.e., communication portion with non-programmable or fixed or non-configurable circuits) or vice versa, wherein such communication portion is selectable or configurable by the designer/system builder as discussed in the rejection of claim 1, including having a plurality of circuit blocks that each provides different data communication functions (as per claim 16) (see rejections of claims 1 and 6 above).

As per **claims 18-20**, all of the elements of claim 15, from which the claim depends, are discussed in the rejection of claim 15 above, wherein the block converter circuit for decoding/encoding and de-scrambling/scrambling circuit for descrambling/scrambling data values corresponds at least to up/down frequency converter, modulator/demodulator block, frequency-hopping spread-spectrum modulator/demodulator block which perform their respective functions in accordance to the data and instructions received (i.e., operational control values) (see col. 7, lines 8-55), wherein such data words are within the scope of the invention as part of the data transmission in the computer systems since such data transmission are usually transferred in blocks of words (i.e., more than one bit at a time) to reduce the amount of time required to complete data transmission.

As per **claim 21**, the programmable logic portion (i.e., block 26') and serial data communication functions (i.e., block 32, Serial Data I/O or SIO) being on a communication portion of the integrated circuit (i.e., block 30), are illustrated in Fig. 2, wherein since the communication portion is non-programmable or non-configurable (abstract; col. 6, lines 51-63; col. 3, lines 20-40), they are accordingly non-synthesizable with the programmable logic device configuration data, wherein since the apparatus/system adapts the non-programmable functional block for performing a function or predetermined function (i.e., SIO for serial data communication function as predetermined by ASIC manufacturer to include this non-programmable block) (col. 4, lines 59-61; col. 6, lines 51-63; col. 5, lines 50-55) and permits the system builder to program the programmable logic portion 26' to perform a desired function (col. 7, lines 1-7; col. 4, line 61 to col. 5, 8), the method and steps for actually performing the predetermined logic functions on the programmable logic portion and for performing serial data communication functions on the communication portion are inherently included in order to arrive at the desired functionalities of the integrated circuit (i.e., ASIC device) and/or to make use of the integrated circuit.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang** (US Patent No. 5,687,325) in view of **Freedman** (US Patent No. 3,851,258).

As per **claim 4**, **Chang** discloses all of the elements of claim 2, from which the claim depends, as discussed in the rejection of claim 2 above, including several timing circuits such as event timers, system timers, real-time clock, clock synthesizer (see Figs. 1 and 2). However, **Chang** fails to teach that these timing circuits receives a clock signal and generates an internal clock signal that is phase shifted with respect to the clock signal. **Freedman** teaches a circuit for producing several phase shifted clocks (i.e.. slower frequency clocks) from the input master clock for use in events timing (see col. 1, lines 6-40). It would have been obvious to one of ordinary skilled in the art at the time of the invention, to further incorporate the particular events timing circuit as taught by **Freedman** into at least one of the timing circuits used in the method/system/apparatus of **Chang** because such incorporation would allows the various components of **Chang** to properly synchronize with one another and/or with the higher frequency central processing system clock, as intended by **Chang**.

10. **Claims 8,22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang** (US Patent No. 6,260,087) in view of **Tzukerman et al.** (US Patent No. 6,724,829).

As per **claims 8,22-23**, **Chang** discloses all of the elements of claims 6,21, from which the respective claims depend, as discussed in the rejection of claims 6,21 above, including the use of encryption/decryption, modulation/demodulation (i.e., scrambling,

encoding, decoding, de-scrambling) on the serial data communication, including in response to the instructions or data streams received (i.e., operational control value or operational control store instruction) (col. 6, line 58 to col. 7, line 55). However, **Chang** fails to teach the particular scrambling/encrypting/encoding involving polynomial-based scrambler circuit and involving the selection of polynomial function values use for scrambling the serial data and encoding the serial data having words of a first bit length into a serial data having words of a second bit length that is different than the first bit length, as claimed. Such scrambling/encryption/encoding is taught in **Tzukerman et al.** (see col. 3, line 66 to col. 4, line 28) to provide for data transmission involving the use of computer systems on cable network which includes advantages such as constant average power level from data burst to data burst, even when different modulation types, are maintained, and the data transmission system, such as a cable modem, can share a transmission channel and a power amplification circuit with other systems without cutting into the power allocated to the other systems (col. 1, lines 10-19; col. 2, lines 40-64), wherein polynomial values are randomly selected by the pseudorandom generator for such scrambling. It would have been obvious to one of ordinary skilled in the art at the time of the invention, to further incorporate the particular scrambling/encrypting/encoding as taught by **Tzukerman et al.** into the method/system/apparatus of **Chang** because such incorporation would allow the serial data communication portion of **Chang** to be able to communicate to other devices or systems on other computer systems via cable network while benefiting from the

advantages of the particular scrambling/encrypting/encoding as taught by **Tzukerman et al.**.

11. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang** (US Patent No. 5,687,325) in view of **Tzukerman et al.** (US Patent No. 6,724,829).

As per **claim 10**, **Chang** discloses all of the elements of claim 9, from which the respective claims depend, as discussed in the rejection of claim 9 above, including the various bus interfaces (see col. 4, line 62 to col. 5, line 13). However, **Chang** fails to teach the particular scrambling/encrypting/encoding involving polynomial-based scrambler circuit and involving the selection of polynomial function values use for scrambling the serial data and encoding the serial data having words of a first bit length into a serial data having words of a second bit length that is different than the first bit length, as part of the communication portion (i.e., via the various bus interfaces) as claimed. Such scrambling/encryption/encoding using a bus interface (i.e., serial link) is taught in **Tzukerman et al.** (see col. 3, line 66 to col. 4, line 28) to provide for data transmission involving the use of computer systems on cable network which includes advantages such as constant average power level from data burst to data burst, even when different modulation types, are maintained, and the data transmission system, such as a cable modem, can share a transmission channel and a power amplification circuit with other systems without cutting into the power allocated to the other systems (col. 1, lines 10-19; col. 2, lines 40-64), wherein polynomial values are randomly selected by the pseudorandom generator for such scrambling. It would have been obvious to one of ordinary skilled in the art at the time of the invention, to further

incorporate the particular scrambling/encrypting/encoding as taught by **Tzukerman et al.** into the method/system/apparatus of **Chang** because such incorporation would allow the communication portion using one of the bus interfaces of **Chang** to be able to communicate to other devices or systems on other computer systems via cable network while benefiting from the advantages of the particular scrambling/encrypting/encoding as taught by **Tzukerman et al.**.

12. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang** (US Patent No. 5,687,325) in view of **Devanagundy et al.** (US Patent No. 6,148,384).

As per **claim 11**, **Chang** discloses all of the elements of claim 9, from which the claim depends, are discussed in the rejection of claim 9, wherein since operational control store (i.e., register file) discussed in the rejection of claim 9, receives its value from the execution of the computer program by the CPU which is directly or indirectly under the control of the user (col. 6, line 66 to col. 7, line 5), the criterion for providing at least one user operational value configured by a user is satisfied. Furthermore, **Chang** also discloses at least the configuration data (i.e., operational values) stored in PROM are preset operational values because they involve data being stored prior to operation of the integrated circuit device (i.e., the integrated circuit devices load the configuration data from PROM) (col. 5, lines 54-65). However, **Chang** fails to teach that such storing configuration data in PROM is done during at least one integrated circuit manufacturing step **Devanagundy et al.** teach the configuration data stored in non-volatile memories, such as ROM, PROM, EPROM, EEPROM, or flash memories, are performed during the manufacture of the circuit, with the advantages such as

including the ease with which the memory can be programmed with configuration data during circuit manufacture, the ability to change configuration data without changing components, and the flexibility of being able to store and alter non-critical data in the same memory containing the configuration data (col. 1, lines 10-34). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further store the operational values (i.e., configuration data) of **Chang** during the manufacturing step as taught by **Devanagundy et al.** because PROM memory used by **Chang** have the advantage of easily stored/programmed during the manufacturing of the circuit while providing the flexibility of being able to store and alter non-critical data in the same memory containing the configuration data as taught by **Devanagundy et al.**.

13. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang** (US Patent No. 5,687,325) in view of **Beal et al.** (US Patent No. 6,791,353).

As per **claim 12**, **Chang** disclose all of the elements of claim 6, from which the claim depends, as discussed in the rejection of claim 6 above. However, **Chang** failed to teach the use of a data (MUX) multiplexer to enable the various input/output data paths as part of the communication portion. **Beal et al.** teach the use of data (MUX) multiplexer for controlling/enabling the various input/output data paths selection for the circuit containing programmable portions mixed with the fixed or non-programmable or specialized circuit portions (see col.3, lines 14-27; col. 8, lines 23-65). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the specialized circuit such as the multiplexer circuit as taught **Beal et al.** to

the manufactured (i.e., fixed or non-programmable or specialized) communication portion of **Chang** because such incorporation would provide for a simple means for circuit paths selection as taught by **Beal et al.** and would provide the circuit needed by **Chang** for configuring/selecting the various circuits datapaths.

Remarks

14. The objection of **claim 10** due to the noted informalities are withdrawn in light of Applicant's amendment to the claims filed on 2/8/2005, which corrected the informalities. However, as per **claim 11**, Applicant's amendment corrected only one of the two informalities noted. Accordingly, the claim remains objected to.

15. The rejections of **claims 1-20** under 35 U.S.C. 102(e) as being anticipated by **Miller** (US Patent No. 6,181,164), are withdrawn in light of Applicant's arguments that the corresponding communication portion (i.e., parity generator, Gold code generator, code scrambler) are not "manufactured to perform a predetermined data communication function or different functions" as claimed, but are rather configured from the configurable elements of the FPGA.

16. The rejections of **claims 21-23** as being unpatentable over **Killian et al.** (US Patent Application Publication No. 2003/0208723) and over **Killian et al.** (US Patent Application Publication No. 2003/0208723) in view of **Miller** (US Patent No. 6,181,164) are withdrawn in light of Applicant's arguments filed on 2/8/2005, wherein as pointed out by Applicant, **Killian et al.** failed to teach the communication portion being manufactured to perform a predetermined data communication function or differences on the same integrated circuit device as claimed.

17. As per **claims 1-23**, the claims are unpatentable over the new grounds of rejections are given above, taking into consideration of Applicant's arguments.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(571) 273-1895 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

Phallaka Kik
U.S. Patent Examiner
April 14, 2005